NANO LETTERS

2007
Vol. 7, No. 4
965−969

Ultralong Single-Crystal Metallic Ni_2Si Nanowires with Low Resistivity

Yipu Song, Andrew L. Schmitt, and Song Jin*

Department of Chemistry, University of Wisconsin—Madison, Madison, Wisconsin 53706

Received December 29, 2006; Revised Manuscript Received March 1, 2007

ABSTRACT

Ultralong, single-crystal Ni_2Si nanowires sheathed with amorphous silicon oxide were synthesized on a large scale by a chemical vapor transport (CVT) method, using iodine as the transport reagent and Ni_2Si powder as the source material. Structural characterization using powder X-ray diffraction, electron microscopy, and energy-dispersive spectroscopy shows that the nanowires have Ni_2Si–SiO_x core–shell structure with single-crystal Ni_2Si core and amorphous silicon oxide shell. The oxide shell is electrically insulating and can be removed by HF etching. Four-terminal electrical measurements show that the single-crystal nanowire has extremely low resistivity of 21 $\mu\Omega$·cm and is capable of supporting remarkably high failure current density >10^8 A/cm^2. These unique Ni_2Si nanowires are very attractive nanoscale building blocks for interconnects and fully silicided (FUSI) gate applications in nanoelectronics.

To sustain the miniaturization of complementary metal oxide semiconductor (CMOS) devices beyond the nanoelectronics regime, more novel materials are incorporated into the transistor structures.[1,2] Among them, transition metal silicides such as nickel silicides have played critical roles as both ohmic contacts and interconnects to CMOS transistors.[2−4] Although not as prominent as NiSi, which is the current contact material of choice for ohmic contact to silicon CMOS, Ni_2Si recently has also been receiving increased attention as the fully silicided (FUSI) metal gates to replace the current polysilicon gates for the future 45 nm CMOS device node and beyond due to absent polydepletion effects, low resistance, and suitable tunable work functions.[5,6] Particularly for p-MOS applications, metal-rich silicides, specifically Ni_2Si, are most suitable because of its attractive work function (∼4.8 eV).[7,8] In such extremely scaled CMOS transistors, nickel silicide materials will have practical cross sections below 50 nm, i.e., in the form of nanowires, via top down lithographic fabrication. An alternative approach to nanoelectronics could be using bottom-up assembled 1-D nanowires (NWs)[9] and cross nanowire structures as functional nanosystems to realize universal computing.[10−14] Following such a paradigm, many nanoelectronic devices[14−16] have been demonstrated using chemically synthesized semiconductor NWs, where heavily doped silicon NWs were usually used as the cross-gate NWs. If the challenges of large-scale hierarchical assembly[10] and precise positioning of NWs can be satisfactorily addressed, nanoscale building blocks of low-resistivity single-crystal metallic materials with a suitable work function such as Ni_2Si will serve as superior interconnects and gate nanowires for crossed NW nanoelectronic architectures.

Part of the challenge to a rational synthesis of Ni_2Si nanowire is the fact that there are six stable nickel silicide phases at room temperature.[17] The first type of credible free-standing nickel silicide nanowires reported, NiSi, was prepared by converting silicon nanowires coated with evaporated nickel film via an annealing process reminiscent of the self-aligned silicidation (SALICIDE) method used in the CMOS process.[18] It was reported that nanowires of this and other nickel silicides were formed by simply decomposing silane gas[19,20] or sputtering silicon[21] on Ni surfaces, although it is unclear how Ni:Si stoichiometry was controlled (2:1, 1:1, or 1:2) throughout the NWs and why silicon nanowires were not formed instead because Ni was a known vapor−liquid−solid (VLS) catalyst for silicon nanowire growth.[9,22] By combining sidewall transfer lithography with self-aligned silicidation, polycrystalline Ni_2Si "nanowires" were also lithographically fabricated on silicon substrate and found to have extremely low resistivity.[23] In this letter, we report a chemical vapor transport method to control the stoichiometry and phase of the silicide nanowires for direct chemical synthesis of ultralong single-crystal Ni_2Si nanowires sheathed with silicon oxide. The resulting Ni_2Si NWs were structurally characterized and found to have a low resistivity and a remarkable failure current density, making them very attractive for gate and interconnect applications.

Silicides are usually refractory materials with high melting points, for example, the mp for Ni_2Si is 1306 °C.[17] Simply heating the silicide solids[24] is not very effective in delivering the materials with sufficient vapor pressures to enable vapor-

* Corresponding author. E-mail: jin@chem.wisc.edu.

10.1021/nl0630687 CCC: $37.00
Published on Web 03/27/2007

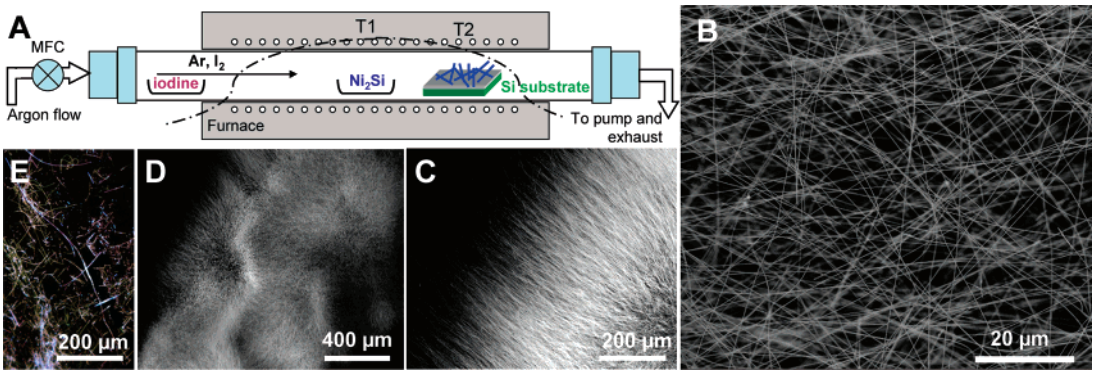

Figure 1. (A) Schematic setup for the synthesis of Ni_2Si nanowires using chemical vapor transport (CVT). (B−D) Representative SEM images of large amounts of as grown Ni_2Si nanowires found on substrates at various magnifications. (E) Dark field optical image of Ni_2Si nanowires dispersed on a silicon substrate highlighting up to 1 mm nanowire length.

phase synthesis of NWs. We have previously succeeded in synthesizing FeSi and CoSi NWs using single source precursors.[25,26] However, analogous organometallic compounds containing nickel that appear suitable as the precursors for vapor synthesis of Ni_2Si NWs are not readily available. In this letter, we have developed a chemical vapor transport (CVT) approach to deliver the gaseous precursors, which will be generally applicable for the vapor-phase synthesis of a wide range of nanowire materials with low vapor pressures. CVT, an established solid-state chemistry technique for growing single crystals,[27] utilizes the reversible thermodynamics commonly observed for many reactions that involve gaseous reactant (the transport reagent, often halogens) and products. Specifically, for the CVT synthesis of silicide nanowires, we used iodine (I_2) as the transport reagent in a home-built continuous flow chemical vapor transport (CVT) reactor comprised of a sealed 1 in. quartz tube placed in a single-zone split tube furnace (Lindberg\Blue M), as illustrated in Figure 1A. At higher temperature ($T_1 = 1000$ °C), iodine reacts with solid powders of silicides to produce gaseous products of metal iodide and silicon iodide that are carried downstream by the inert argon gas flow to a different temperature zone ($T_2 \approx 850$ °C), where the thermodynamics of reaction reverses. Here the reaction proceeds in the reverse direction and gives back the target silicide along with iodine:

$$Ni_2Si(s) + 4\ I_2(g) \leftrightarrow 2\ NiI_2(g) + SiI_4(g)$$

In a typical NW synthesis reaction, iodine powder (2.5 g) in an alumina boat was placed upstream just outside of the tube furnace, Ni_2Si powder (2.0 g from Alfa Aesar, usually 20−30 mg was consumed) in an alumina boat was placed in the center of a tube furnace, whereas Si/SiO_2 substrates, on which several drops of aqueous $Ni(NO_3)_2$ solution (0.1 M) have been dispersed and air-dried, were placed downstream in the heating zone. The tube reactor was flushed with argon at 20 sccm for 30 min, and then heated to 1000 °C (temperature at the center) for 4 h under argon flow (20 sccm) and atmospheric pressure, followed by a natural cooldown. Dark-gray layers of fluffy materials, often extending from the substrate surfaces up to a few millimeters in height, were clearly visible to unaided eyes on the substrates. The

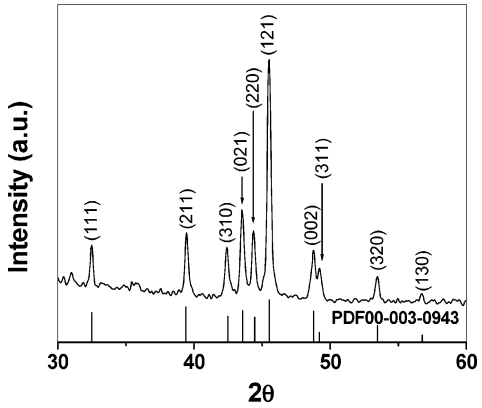

Figure 2. Powder X-ray diffraction pattern from a sample of Ni_2Si nanowires covering the growth substrate.

morphology of the as-grown products was examined using field emission scanning electron microscope (SEM, LEO SUPRA 1530). Representative scanning electron microscopy (SEM) image (Figure 1B) revealed smooth and straight nanowires of mostly 30−80 nm in diameter produced in high yield. Large amounts of NWs with a typical length of several hundred micrometers even up to millimeters were routinely produced, as seen in the low-magnification SEM images (Figure 1C and D). When the NWs were dispersed in ethanol by ultrosonication and then deposited on silicon substrates, some NWs as long as 1 mm were still clearly visible in dark-field optical images (Figure 1E) despite the mechanical destruction. The best nanowire growth in terms of morphology and yield was observed for substrates located in the temperature range of 820−870 °C.

The copious amount of NWs produced permitted us to readily characterize the product using powder X-ray diffraction (PXRD), as shown in Figure 2. All major diffraction peaks can be matched to that of the orthorhombic phase of δ-Ni_2Si (JCPDS PDF00-003-0943) (Space group *Pbnm*, no. 62, Pearson symbol *oP*12).[28,29,30] The calculated lattice parameters from PXRD data, $a = 7.068$ Å, $b = 5.004$ Å, and $c = 3.722$ Å, are in good agreement with the literature. No other nickel silicide phases or other crystalline impurity phases were detectable by PXRD, which highlights the rational control of Ni:Si stoichiometry afforded by our CVT methods.

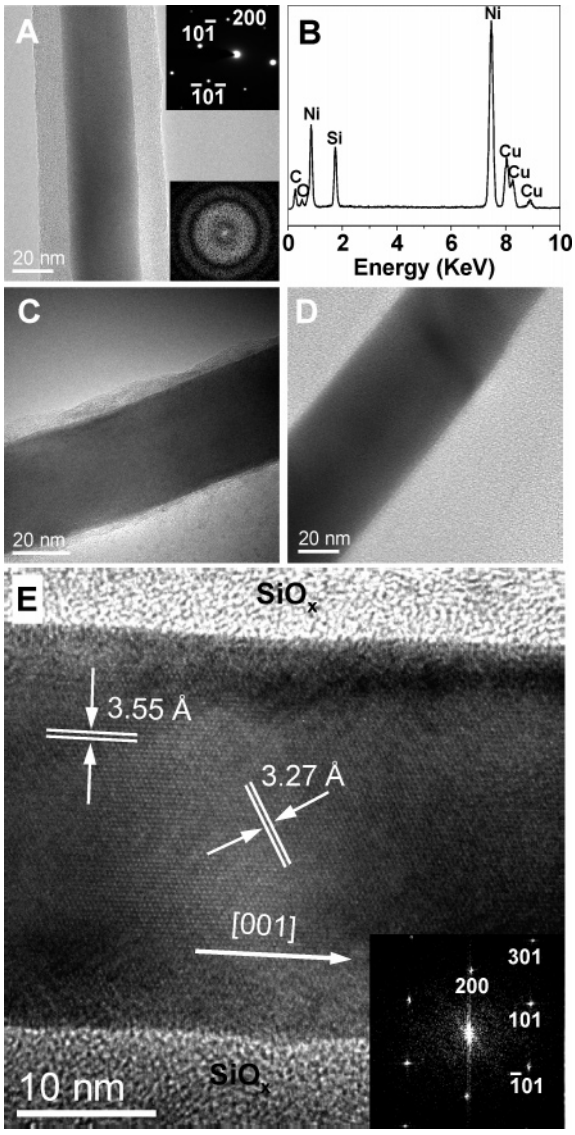

Figure 3. (A) Representative low-magnification TEM image of a Ni_2Si nanowire. The upper inset shows the SAED pattern of the NW core along the [010] zone axis, the lower inset shows the SAED pattern of the NW shell. (B) EDS spectrum of the corresponding nanowire. (C−D) Low-magnification TEM image of Ni_2Si nanowires observed immediately after etching in buffer HF for 10 s (C) and 20 s (D). (E) Representative HRTEM image of a Ni_2Si nanowire along the [010] zone axis and the corresponding two-dimensional FFT (inset).

The Ni_2Si NWs were further characterized using transmission electron microscopy (TEM). The as-grown NWs were sonicated and suspended in ethanol, dispersed onto TEM grids with lacey carbon film, and imaged with a Philips CM200 TEM with an accelerating voltage of 200 kV. A representative low-magnification TEM image of a typical NW (Figure 3A) reveals that the NWs have an inner core and an outer shell structure. The selected area electron diffraction (SAED) patterns recorded from the core region (upper inset of Figure 3A) reveal the single crystallinity of the core and can be indexed to the orthorhombic Ni_2Si structure along the [010] zone axis. The ED patterns do not change as the electron beam is moved along the NW axes, indicating single-crystal structure. The SAED patterns taken for the outer shell region (lower inset of Figure 3A) show dispersed circles, indicating an amorphous phase. The chemical composition of the nanowires was analyzed by energy-dispersive spectroscopy (EDS). As shown in Figure 3B, the EDS spectrum reveals that the nanowire consists of Ni, Si, and O elements in the atomic ratios of Ni:Si:O = 56:29:15 (Cu and C are from the TEM grid), which is close to Ni:Si = 2:1 within the errors of EDS analysis. EDS analysis at different positions of the NWs along the axial directions show no noticeable change in compositions. Elemental line-scan analysis along the radial direction of NWs shows that there are Si and O in approximate atomic ratio 3:7 in the shell region and Ni, Si, and O in approximate atomic ratios of 5:3:2 over the core region, which suggests that the outer amorphous shell only consists of silicon oxide (SiO_x). The shell thickness is about 10−20 nm for most of nanowires. This oxide layer can be removed by progressively longer etching in buffer HF, as shown in Figure 3C (10 s) and Figure 3D (20 s), until the oxide is completely removed (the TEM was performed immediately after the etching). Furthermore, when NWs were treated by HF etching and then kept in ambient environment at room temperature for two weeks, significant reoxidization of more than several nanometers was *not* observed on the NW surface. This suggests that the oxide shell should be formed during the high-temperature nanowire synthesis process in which a trace amount of oxygen could be present in the simple CVT setup employed. It is generally understood that surface oxidation of silicides produces silicon oxide,[31] and Ni_2Si was believed to have more facile oxidation compared with other silicides.[32]

High-resolution TEM (HRTEM) image (Figure 3E) of a representative unetched Ni_2Si NW clearly shows lattice fringes of a single-crystal nanowire with about 30 nm core diameter along the [010] zone axis. The measured lattice spacings observed in HRTEM are 3.55 and 3.27 Å, corresponding well to the (200) and (101) lattice spacings of the orthorhombic Ni_2Si structure, respectively. The two-dimensional fast Fourier transform (FFT) of the lattice-resolved image (inset of Figure 3E) shows the reciprocal lattice peaks, which can be indexed to a primitive orthorhombic lattice. Indexed reciprocal lattices observed show that about half of the NWs have growth axes parallel to the [001] crystallographic directions, but [010] and other directions are observed as well.

The presence of minute amounts of $Ni(NO_3)_2$ is crucial to the formation of large amounts of NWs. It is plausible that the nanowire growth is through the vapor−liquid−solid (VLS) or related mechanism on the basis of the Ni-rich side of Ni−Si phase diagram,[17] where Ni can be the catalyst for the formation of Ni_2Si NWs. However, no apparent catalytic caps were observed at the end of NWs in microscopy examination, and the growth temperature employed (820−870 °C) is lower than the eutectic temperature. It is likely that trace amount of Ni (from $Ni(NO_3)_2$) provides initial nucleation sites for the incoming Ni and Si in a 2:1 ratio delivered by CVT thereby facilitates Ni_2Si NW formation, but it participates in the later growth reaction and is not noticeably present in the end products. Such metal-assisted

NW growth has often been observed before, for example, in oxide[24] and GaN NW growth.[9] We also want to emphasize that the amount of Ni from $Ni(NO_3)_2$ is definitely not sufficient for the observed large-scale Ni_2Si NW growth based on a simple estimate. In a typical CVT reaction, the transport reagent iodine reacts with about 20−30 mg Ni_2Si powder at high temperature, and the resulting precursors were delivered to supply the nickel and silicon for nanowire growth at lower temperature. Notably, if the transport reagent iodine was not used in the reactions under otherwise identical conditions, no products of any form were ever observed on the substrates, highlighting the critical role CVT plays in the synthesis of silicide NWs. We believe it is generally possible to use the CVT method to deliver stoichiometrically controlled precursors using corresponding source materials and suitable CVT reaction conditions to synthesize NWs of other nickel silicides, such as NiSi or Ni_3Si, so long as catalytic formation of nanowires can be enabled.

To investigate the electrical properties of these single-crystal Ni_2Si NWs, we fabricated four-terminal NW devices using a standard e-beam lithography technique. For contacting to the NWs, the samples were etched in buffer HF solution for various times to remove the oxide layer, rinsed in DI water for 20 s, and dried in a nitrogen flow right before the deposition of the Ti/Au metal electrode by e-beam evaporation. Adequate HF etching is critical to making electrical contact: $I-V$ measurements for the Ni_2Si NW devices that were subjected to HF etching for 10 s or less showed no conductivity. Recall that, in the TEM studies (Figure 3C), NWs still have a noticeable 2−5 nm silicon oxide layer after a 10 s HF treatment. The oxide shell is clearly a good electric insulator. TEM showed that a 20 s HF treatment removed all insulating layers (Figure 3D), and indeed, a 20 s HF etching before metal contact produced nearly quantitative yields of conducting devices. For properly etched Ni_2Si NW devices, the current (I) versus voltage (V) curves display a perfect linear $I-V$ behavior, as shown for a representative device in Figure 4A. The current was extremely high, often exceeding 100 μA at a voltage of 100 mV. Such low resistivity means that the contact resistance, if not properly accounted for, could dominate the observed transport behavior. Four-terminal $I-V$ measurements were conducted by driving a known current between the two outermost contacts, while the potential difference was measured between the two inner contacts (Figure 4A inset). Two- (red line 1 in Figure 4A) and four-terminal (blue line 2) $I-V$ measurements yielded resistances of 2.01 kΩ and 703 Ω , respectively, for this 3.2 μm long Ni_2Si NW device with a core diameter of 34 ± 1 nm, which corresponds to the low resistivity of 57 ± 2 $\mu\Omega$·cm and 20 ± 1 $\mu\Omega$·cm for two- and four-terminal measurements, respectively. Measurements for ten devices gave an average four-terminal resistivity of 21 ± 1 $\mu\Omega$·cm for Ni_2Si NWs. This resistivity value is lower than both the thin film resistivity of Ni_2Si materials (24 $\mu\Omega$·cm)[33] and that reported for recently observed polycrystalline Ni_2Si "nanowire" before annealing treatment (25 $\mu\Omega$·cm),[23] which should be attributed to the single-crystal structure in our case. This is only twice as resistive as the most conducting silicide, NiSi, which has resistivity of 10 $\mu\Omega$·cm in thin film[33] and in nanowire form.[18,21] Temperature-dependent measurement (Figure 4B) shows that the nanowire resistance decreases monotonically down to about 20 K and then saturates. This kind of temperature dependence is the typical behavior expected for the resistance of a normal metal,[33] confirming the metallic nature of Ni_2Si NWs.

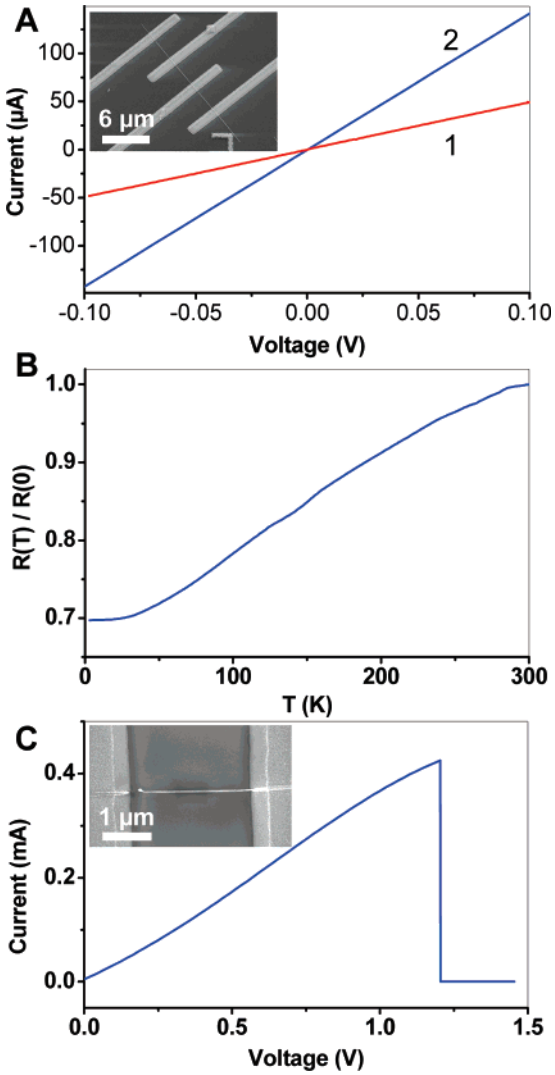

Figure 4. Transport measurements on individual single-crystal Ni_2Si nanowire. (A) Room-temperature current vs voltage curves recorded for a four-terminal device made of a Ni_2Si nanowire with a core diameter of 34 nm and overall diameter of 48 nm, with red line (1) and blue line (2) corresponding to two- and four-terminal measurements, respectively. Inset: SEM image of the device measured. (B) Temperature-dependent normalized four-terminal resistance of individual Ni_2Si nanowire; the resistance, $R(T)$, is normalized by the value at 300 K, $R(0)$. (C) Current vs voltage recorded for a typical Ni_2Si NW device that breaks down at higher voltage and current. Inset: SEM image of this particular device after failure.

The maximum transport current density (J_{max}) was also characterized for the metallic Ni_2Si NWs using two-terminal measurements. Typically, NW devices break down at current level of 0.4−0.6 mA when voltages are above 1.2 V (two-terminal measurements). Figure 4C shows the behavior of a typical device with a core NW diameter of 22 nm that

exhibits a maximum current of 0.427 mA before a precipitous drop to zero at about 1.2 V, which corresponds to a high failure current density (J_{max}) about 1.1×10^8 A/cm^2. The inset of Figure 4C showing this broken nanowire after the breakdown test reveals that the failure occurs at the end point of the nanowire close to the contact, probably owing to resistive self-heating. The fact that the failure did not occur in the middle of silicide NWs as observed previously[18,25,26] suggests that the contact still has higher resistance than the NW body and becomes the hot spot in resistive heating, which might have limited the observed J_{max}. A total of 17 devices were measured for breakdown test, and the maximum current densities (J_{max}) are all greater than 1×10^8 A/cm^2, which is comparable to NiSi NWs[18] and 2 orders of magnitude higher than lithographically defined lines of noble metals[34] and further attests to the high quality of these chemically synthesized Ni_2Si NWs. These low resistivity metallic NWs are attractive 1-D nanoscale building blocks as interconnects and gates in nanoelectronics devices. In complex functional nanosystems, bottom-up assembled cross-nanowire architectures are crucial to the functions of addressable gating, multiplex decoders, configurable memory arrays, and programmable logic functions to realize universal computing.[12−16] Going beyond the NW field-effect transistor arrays using global back gates that are not individually addressable,[35] lithographically defined local gates or heavily doped semiconductor NWs have been used as local cross-gates.[14−16] These unique $Ni_2Si-SiO_x$ core−shell NWs with insulating oxide shell are particularly promising to replace them as nanoscale cross-NW gates, with the insulating oxide layer serving as convenient gate dielectrics. Thus Ni_2Si NWs can serve as "fully silicided" metallic gates for a p-Si nanoFET device based on cross-nanowires of Si and $Ni_2Si-SiO_x$ NWs, for which the gate length can be as small as 20 nm, i.e., the size of the NW cross-points. The appropriate work function of Ni_2Si can reduce the threshold voltage,[6,8] and the high failure current density will ensure robust high-density integration. The copious amount of millimeter long NWs produced by our direct chemical synthesis would enable one to assemble large and dense arrays[10] of crossed nanowire transistors that could enable integrated nanosystems.

In conclusion, large-scale chemical synthesis of ultralong single-crystal Ni_2Si nanowires has been achieved using a chemical vapor transport (CVT) method. Structural characterization indicates that the NWs have $Ni_2Si-SiO_x$ core−shell nanostructure with a single-crystal Ni_2Si core and an insulating amorphous silicon oxide shell. Electrical measurements indicate that the metallic Ni_2Si NWs have a low resistivity of 21 $\mu\Omega$·cm and a remarkable failure current density of at least 1×10^8 A/cm^2. These unique Ni_2Si NWs are attractive nanoscale building blocks for interconnect and fully silicided (FUSI) gate applications in nanoelectronics.

Acknowledgment. This research is supported by a WARF Draper TIF grant. S.J. thanks NSF (CAREER DMR-0548232), 3M Nontenured Faculty Award, and DuPont S&E grant for financial support. We thank Professor Robert J. Hamers for the access to SEM (NSF DMR-0210806) and Professor Mark Eriksson for access to the PPMS.

References

(1) Barrett, C. R. *MRS Bull.* **2006**, *31*, 906.
(2) Leong, M.; Narayanan, V.; Singh, D.; Topol, A.; Chan, V.; Ren, Z. *Materi. Today* **2006**, *9*, 26.
(3) Zhang, S. L.; Smith, U. *J. Vac. Sci. Technol., A* **2004**, *22*, 1361.
(4) Chen, L. J. *Silicide Technology for Integrated Circuits*; The Institution of Electrical Engineers: London, 2004.
(5) Maszara, W. P. *J. Electrochem. Soc.* **2005**, *152*, G550.
(6) Kittl, J. A.; Lauwers, A.; Pawlak, M. A.; van Dal, M. J. H.; Veloso, A.; Anil, K. G.; Pourtois, G.; Demeurisse, C.; Schram, T.; Brijs, B.; De Potter, M.; Vrancken, C.; Maex, K. *Microelectron. Eng.* **2005**, *82*, 441.
(7) Pawlak, M. A.; Lauwers, A.; Janssens, T.; Anil, K. G.; Opsomer, K.; Maex, K.; Vantomme, A.; Kittl, J. A. *IEEE Electron Device Lett.* **2006**, *27*, 99.
(8) Kittl, J. A.; Pawlak, M. A.; Lauwers, A.; Demeurisse, C.; Opsomer, K.; Anil, K. G.; Vrancken, C.; van Dal, M. J. H.; Veloso, A.; Kubicek, S.; Absil, P.; Maex, K.; Biesemans, S. *IEEE Electron Device Lett.* **2006**, *27*, 34.
(9) Xia, Y.; Yang, P.; Sun, Y.; Wu, Y.; Mayers, B.; Gates, B.; Yin, Y.; Kim, F.; Yan, H. *Adv. Mater.* **2003**, *15*, 353.
(10) Whang, D.; Jin, S.; Wu, Y.; Lieber, C. M. *Nano Lett.* **2003**, *3*, 1255.
(11) Beckman, R.; Johnston-Halperin, E.; Luo, Y.; Green, J. E.; Heath, J. R. *Science* **2005**, *310*, 465.
(12) DeHon, A. *IEEE Trans. Nanotechnol.* **2003**, *2*, 23.
(13) Snider, G.; Kuekes, P.; Hogg, T.; Williams, R. S. *Appl. Phys. A* **2005**, *80*, 1183.
(14) Zhong, Z. H.; Wang, D. L.; Cui, Y.; Bockrath, M. W.; Lieber, C. M. *Science* **2003**, *302*, 1377.
(15) Huang, Y.; Duan, X. F.; Cui, Y.; Lauhon, L. J.; Kim, K. H.; Lieber, C. M. *Science* **2001**, *294*, 1313.
(16) Li, Y.; Qian, F.; Xiang, J.; Lieber, C. M. *Mater. Today* **2006**, *9*, 18.
(17) Okamoto, H. *Desk Handbook: Phase Diagrams for Binary Alloys*; ASM International: Materials Park, OH, 2000.
(18) Wu, Y.; Xiang, J.; Yang, C.; Lu, W.; Lieber, C. M. *Nature* **2004**, *430*, 61.
(19) Dong, L. F.; Bush, J.; Chirayos, V.; Solanki, R.; Jiao, J. *Nano Lett.* **2005**, *5*, 2112.
(20) Yan, X. Q.; Yuan, H. J.; Wang, J. X.; Liu, D. F.; Zhou, Z. P.; Gao, Y.; Song, L.; Liu, L. F.; Zhou, W. Y.; Wang, G.; Xie, S. S. *Appl. Phys. A* **2004**, *79*, 1853.
(21) Kim, J.; Anderson, W. A. *Nano Lett.* **2006**, *6*, 1356.
(22) Wagner, R. S.; Ellis, W. C. *Trans. Metall. Soc. AIME* **1965**, *233*, 1053.
(23) Zhang, Z.; Lu, J.; Hellstrom, P. E.; Ostling, M.; Zhang, S. L. *Appl. Phys. Lett.* **2006**, *88*, 213103.
(24) Pan, Z. W.; Dai, Z. R.; Wang, Z. L. *Science* **2001**, *291*, 1947.
(25) Schmitt, A. L.; Zhu, L.; Schmeier, D.; Himpsel, F. J.; Jin, S. *J. Phys. Chem. B* **2006**, *110*, 18142.
(26) Schmitt, A. L.; Bierman, M. J.; Schmeisser, D.; Himpsel, F. J.; Jin, S. *Nano Lett.* **2006**, *6*, 1617.
(27) West, A. R. *Solid State Chemistry and its Applications*; Wiley & Sons: Chichester, U.K., 1984; p 21.
(28) Villars, P.; Calvert, L. D. *Pearson's Handbook of Crystallographic Data for Intermetallic Phases*, 2nd ed.; ASTM International: Newbury, OH, 1991.
(29) Toman, K. *Acta Cryst.* **1952**, *5*, 329.
(30) There are three equivalent cell settings for space group no. 62: *Pnma*, *Pbnm*, and *Pcma*, all of which are adopted by various literatures such as Pearson's Index (ref 28), JCPDS database, and previous publications (refs 20, 29). Different choices do not change the X-ray or electron diffraction patterns, but affect their indices as the cell axes are swapped. We used the *Pbnm* setting throughout this paper.
(31) Dheurle, F. M.; Cros, A.; Frampton, R. D.; Irene, E. A. *Philos. Mag. B* **1987**, *55*, 291.
(32) Valeri, S.; Delpennino, U.; Lomellini, P.; Ottaviani, G. *Surf. Sci.* **1985**, *161*, 1.
(33) Maex, K.; Van Rossum, M. *Properties of Metal Silicides*; INSPEC, The Institution of Electrical Engineers: London, 1995.
(34) International Technology Road Map for Semiconductors (ITRS), 2005, http://www.itrs.net/Common/2005ITRS/Interconnect2005.pdf.
(35) Jin, S.; Whang, D. M.; McAlpine, M. C.; Friedman, R. S.; Wu, Y.; Lieber, C. M. *Nano Lett.* **2004**, *4*, 915.

NL0630687